WHAT IS CLAIMED IS:

1. A video signal processing device comprising:

a gain controller for gain-controlling a digitalized video signal per minimum video unit thereof; and

a variation controller for setting video blocks each comprising a plurality of minimum video units and setting a gain control value of the gain controller in each of the minimum video units constituting the set video blocks, wherein

the gain controller serially divides the video signals into the video blocks and gain-controls the respective minimum video units constituting the respective video blocks resulting from the division based on the gain control values.

2. The video signal processing device as claimed in Claim 1, wherein

the variation controller sets a plurality of groups of minimum video units each comprising at least a minimum video unit in the respective video blocks and sets the gain control value in each of the groups of minimum video units.

3. The video signal processing device as claimed in Claim 2, wherein

the video signal is an interlace video signal whose frame period is 1/30 second and minimum video unit is a field, and

the variation controller sets the respective video blocks to include five fields, and the variation controller further sets one of the groups of minimum video units to include first and second fields of the video blocks and sets the other of the groups of minimum video units to include third, fourth and fifth fields of the video blocks.

4. The video signal processing device as claimed in Claim 2, wherein

the video signal is an interlace video signal whose frame period is 1/30 second and minimum video unit is a field, and

the variation controller sets the respective video blocks

to include ten fields, and the variation controller further sets one of the groups of minimum video units to include first, second, sixth, seventh and eighth fields of the video blocks and sets the other of the groups of minimum video units to include third, fourth, fifth, ninth and tenth fields of the video blocks.

5. The video signal processing device as claimed in Claim 2, wherein

the video signal is an interlace video signal whose frame period is 1/30 second and minimum video unit is a field, and

the variation controller sets the respective video blocks to include four fields, and the variation controller further sets one of the groups of minimum video units to include first and second fields of the video blocks and sets the other of the groups of minimum video units to include third and fourth fields of the video blocks.

6. The video signal processing device as claimed in Claim 2, wherein

the video signal is an interlace video signal whose frame period is 1/25 second and minimum video unit is a field, and

the variation controller sets the respective video blocks to include four fields, and the variation controller further sets one of the groups of minimum video units to include first and second fields of the video blocks and sets the other of the groups of minimum video units to include third and fourth fields of the video blocks.

7. The video signal processing device as claimed in Claim 2, further comprising:

a memory for storing the digitalized video signal;

a selector for alternatively selecting one of the video signal and an output of the memory and outputting a result of the selection; and

a memory controller for controlling write of the video signal in the memory, read of the video signal from the memory

and the output of the selector based on a frame synchronous signal of the video signal.

8. The video signal processing device as claimed in Claim 7, wherein

the gain controller gain-controls the output of the selector.

9. The video signal processing device as claimed in Claim 7, wherein

the gain controller gain-controls the video signal and supplies the gain-controlled video signal to the memory and the selector.

10. The video signal processing device as claimed in Claim 7, wherein

the video signal is an interlace video signal whose frame period is 1/30 second and minimum video unit is a field, and

the memory controller sets the respective video blocks to include five fields, and instructs the memory to write first and third fields therein and instructs the selector to selectively output the first and third fields at input timings of the first and third fields of the video blocks, and

the memory controller instructs the memory to read the data stored therein and instructs the selector to selectively output the read output of the memory at input timings of second, fourth and fifth fields of the video blocks.

11. The video signal processing device as claimed in Claim 7, wherein

the video signal is an interlace video signal whose frame period is 1/30 second and minimum video unit is a field, and

the memory controller sets the respective video blocks to include ten fields, and instructs the memory to write first, third, sixth and ninth fields therein and instructs the selector to selectively output the first, third, sixth and ninth fields at input timings of the first, third, sixth and ninth fields

of the video blocks, and

the memory controller instructs the memory to read the data stored therein and instructs the selector to selectively output the read output of the memory at input timings of second, fourth, fifth, seventh, eighth and tenth fields of the video blocks.

12. The video signal processing device as claimed in Claims 4, 5 and 6, wherein

the variation controller synchronizes a bundle of video blocks each equivalent to a second with a frame period of the video signal.